WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array having dynamic memory cells; and

a refresh controller that executes refresh operation for the memory cell array,

wherein the refresh controller comprises:

a refresh timing signal generator that periodically generates a refresh timing signal used to establish a timing of execution of the refresh operation;

a refresh request signal generator that generates a refresh request signal indicating a request for the execution of the refresh operation in response to the refresh timing signal; and

a refresh execution signal generator that generates a refresh execution signal indication the execution of the refresh operation in response to the refresh request signal and another signal,

wherein the refresh request signal generator comprises:

a first counter that counts the number of times the refresh timing signal has been generated; and

a second counter that counts the number of times the refresh execution signal has been generated,

and wherein the refresh request signal generator generates the refresh request signal if a difference between the number of times the refresh timing signal has been generated and the number of times the refresh execution signal has been generated is one or more, and

the refresh execution signal generator is capable of generating two or more of the refresh execution signals within one cycle of the refresh timing signal if the

difference is two or more.

2. The semiconductor memory device according to Claim 1, further comprising:

an external access controller that executes an external access operation with respect to a memory cell specified using an external address that is given by an external device, the external address including a row address and a column address,

wherein if only a predetermined bit included in the column address changes, the external access controller maintains a word line selected by the row address in an active state; and

if the word line is maintained in the active state, the refresh controller delays the generation of the refresh execution signal until a bit other than the predetermined bit included in the external address changes.

3. The semiconductor memory device according to Claim 2,

wherein if the refresh execution signal is delayed two or more times, the refresh controller sequentially generates the refresh execution signals each time the bit other than the predetermined bit included in the external address changes in a first operation mode in which the external access operation is enabled, and continuously generates the refresh execution signals in a second operation mode in which the external access operation is prohibited.

4. The semiconductor memory device according to Claim 1, wherein the number of bits in the second counter is set to match the number of rows included in the memory cell array, and the refresh controller uses an output value from the

second counter as a refresh address to specify a row in the memory cell array.

5. The semiconductor memory device according to Claim 1, wherein the number of bits in the first counter is set to a number smaller than the number of bits in the second counter, and the refresh request signal generator generates the refresh request signal using an output from the first counter and a part of an output from the second counter.

6. The semiconductor memory device according to Claim 1, further comprising:

an internal voltage generator that includes a charge pump circuit and generates internal voltage for the semiconductor memory device using voltage supplied externally,

wherein the internal voltage generator generates the internal voltage using the refresh execution signals supplied from the refresh execution signal generator.

7. The semiconductor memory device according to Claim 6, wherein the refresh controller further comprises:

a setting section that sets the output values from the two counters to different values when power-on processing is executed for the semiconductor memory device,

and wherein the refresh controller continuously generates the refresh execution signals when the power-on processing is executed until the output values from the two counters match.

8. A semiconductor memory device comprising:

an internal voltage generator that includes a charge pump circuit and generates internal voltage for the semiconductor memory device using voltage supplied externally; and

a pulse signal supply section that supplies pulse signals to the internal voltage generator,

wherein the pulse signal supply section comprises:

an output section that outputs a predetermined value when power-on processing for the semiconductor memory device is executed; and

a pulse signal counter that counts the number of times the pulse signal has been generated,

and wherein the pulse signal supply section continuously generates the pulse signals when the power-on processing is executed until an output value from the output section matches an output value from the pulse signal counter.

9. The semiconductor memory device according to Claim 8, wherein the output section comprises:

a periodic signal counter that counts the number of times a predetermined periodic signal has been generated; and

a setting section that sets an output value from the periodic signal counter to the predetermined value,

wherein the semiconductor memory device further comprises:

a memory cell array having dynamic memory cells,

and wherein the periodic signal counter and the pulse signal counter are counters used for the execution of the refresh operation regarding the memory cell array after the power-on processing is completed.